**Lab 3.1.A: Putting opamps to ‘gainful’ use [Negative Feedback]**

All question material is in blue. Please put your answers in black color font.  
Note on symbols for Gain:   
In earlier labs we used the symbol **G** to denote the open-loop gain of an opamp. For the LM741 **G~106**(effectively infinite as approximated in most equations).   
As discussed in class, the opamp working in open-loop mode is not very useful. Our objective is to design and build an opamp circuit with a finite gain – we will call this gain **Gf i.e. the gain with feedback in place. Gf is a finite number whose value is specified by design**

**Part A: Simple Negative Feedback**

**A.1) Simple negative feedback to set finite voltage gain Gf**

**A.1.1 non-inverting negative feedback**In the pre-lab session, the following scheme of negative feedback was discussed to arrange a circuit with gain :

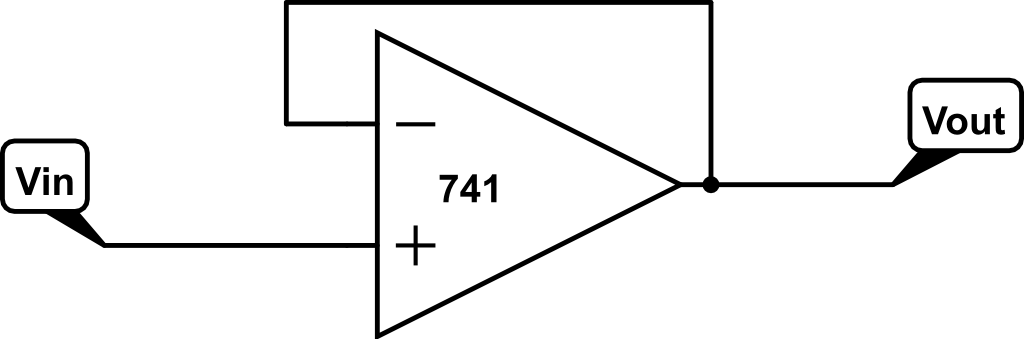


Fig 1: Basic scheme for opamp negative feedback, preserving the sign of

**A.1.1.1) Design [2]**

Arrange a resistor divider to feedback a fraction of the output voltage back to the input of the opamp.

Work out the design equations to calculate values of the resistor divider for in your circuit design. Justify the choice of particular resistor values you use. Write all steps of the design equation here: Use ‘Insert equation’ in MS-Word or Libre-Office to format your equations correctly including subscripts. A prototype equation is provided below, which you may copy-paste and reuse. One equation per line looks good!

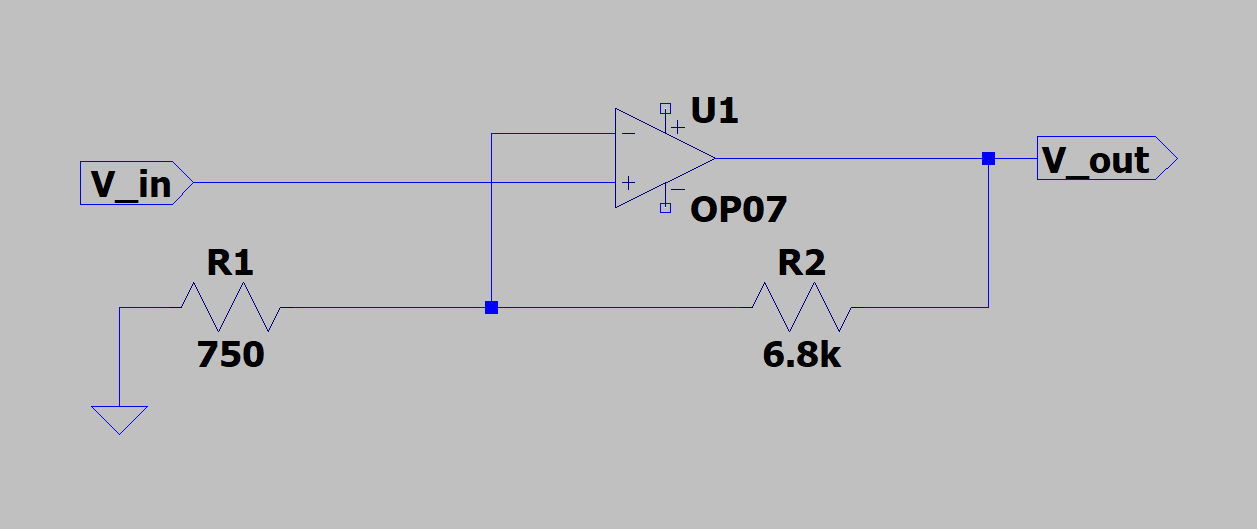
Closed loop gain,

Therefore,

A decent choice of R1 and R2 that satisfies the above relation would be 6.8kΩ and 750Ω respectively.

**A.1.1.2) LTSpice simulation**

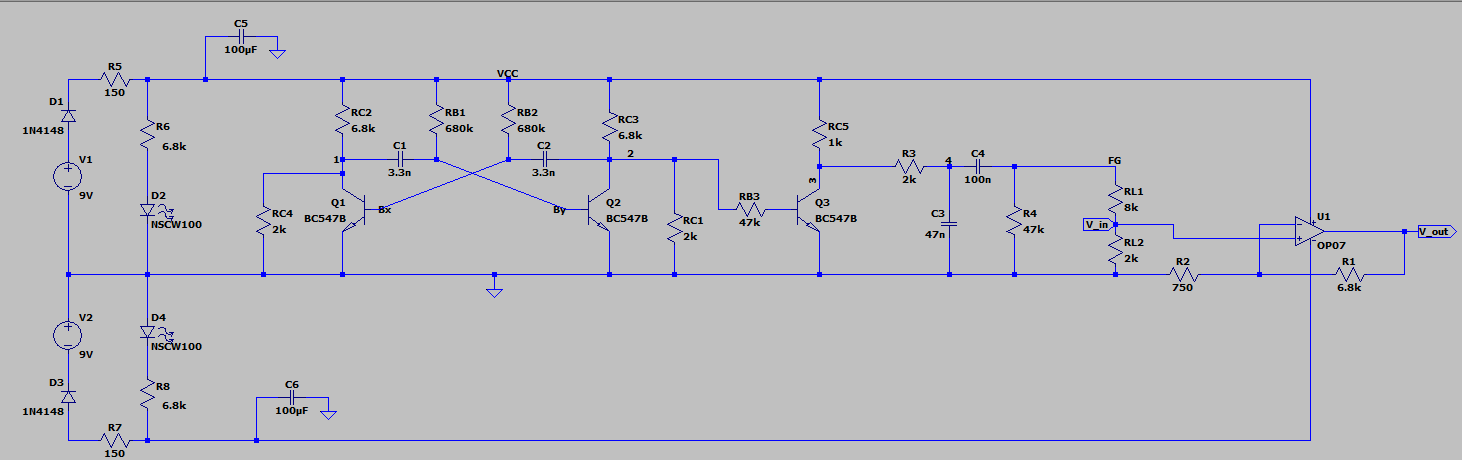
Draw your circuit diagram in LTSpice. **[2]**  
For clarity, only put your negative feedback opamp circuit design here (not full design with FG)   
You may use the standard opamp available in LTSpice OP07 as a stand-in replacement for LM741

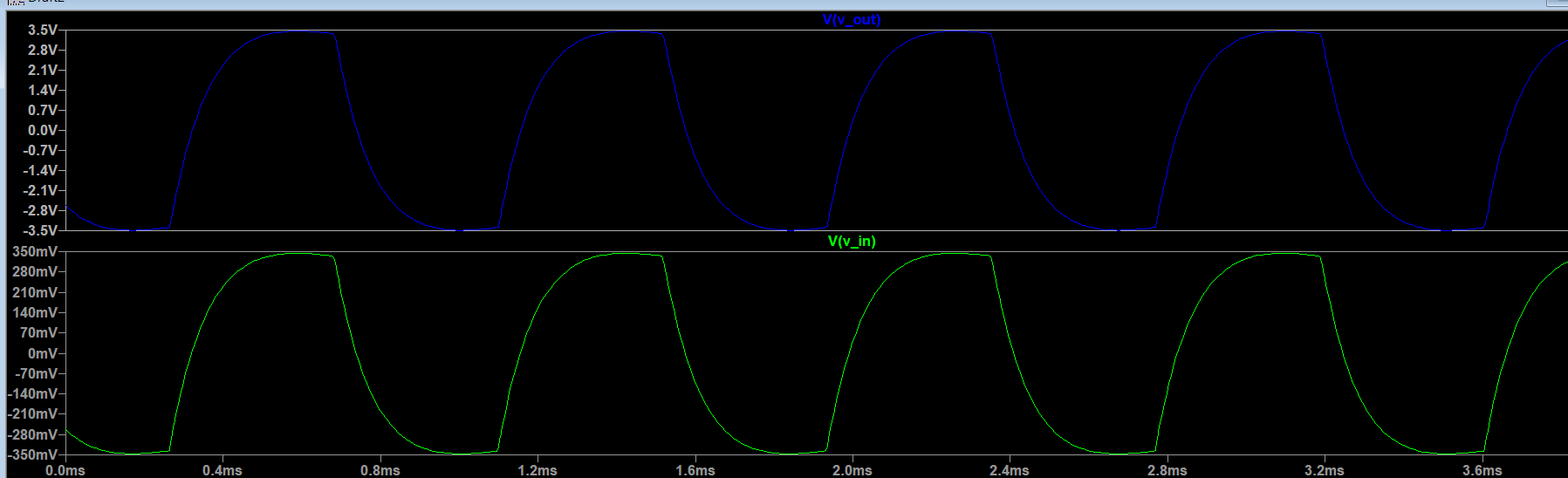


Run the simulation in LTSpice and put below a plot of your simulated Vin → Vout signals.   
Now obviously you need to include the FG simulation for this step.

Remember to put large value electrolytic (100μF/47μF/22μF/10μF) power supply bypass capacitors for both FG and opamp power rails. Note that you will be running the opamp with ≈ ±8V VCC rail voltage as setup in Lab 2. From the simulation determine a suitable amplitude of Vin such that Vout does not hit the opamp saturation voltage limits when you test the circuit experimentally in the next step.Objective of your simulation: Verify the gain and phase difference (if any) in the transfer function

To check the phase difference, you must display both Vin and Vout with individual scaling on Y-axis: First plot just V­in using the voltage probe tool. Then, select the Output window and choose “Add Plot Pane” option from the “Plot Settings” drop-down control. Next, plot Vout as the second voltage using the voltage probe tool **[2]**

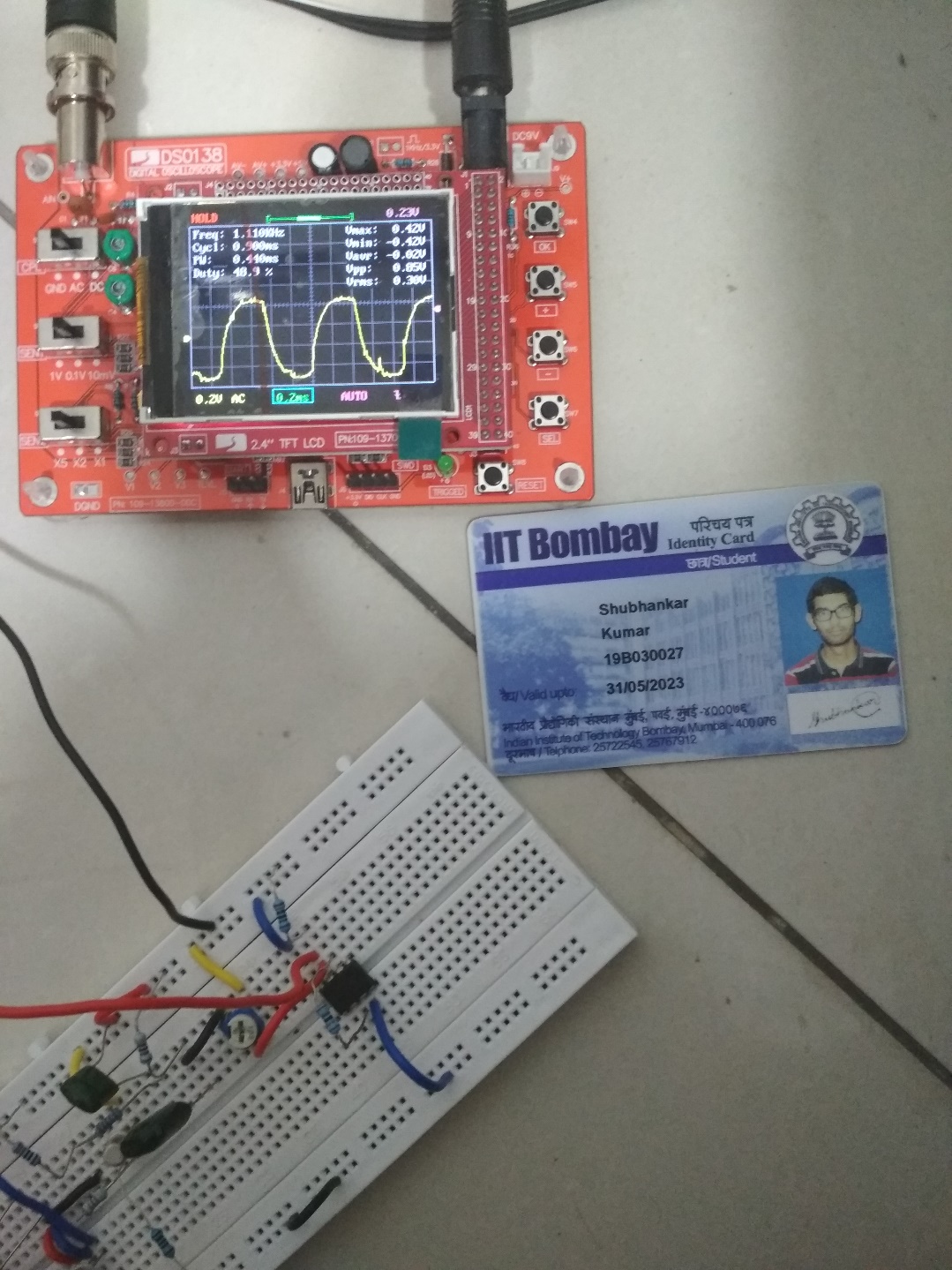
****

****

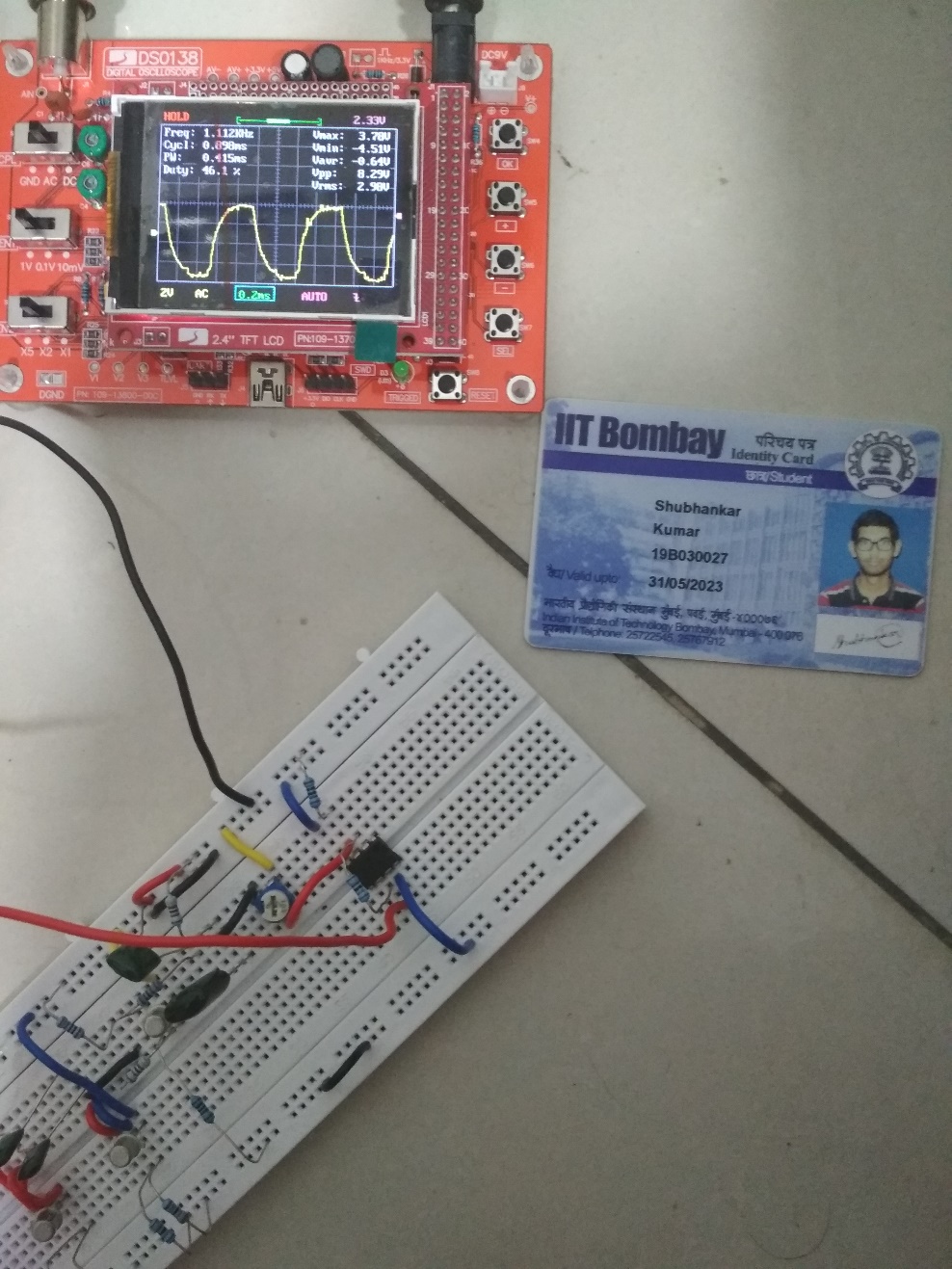
**A.2) Circuit demo: Non-inverting amplifier with**  **[6]**

Build the opamp circuit as designed and simulated in the above steps on your breadboard. Drive the input with the FG used in earlier labs. Set the FG output amplitude as chosen in the simulation.

Put a photo of your working setup here, clearly labelling and . With a single channel DSO measurement, it is not possible to measure the phase difference in experiment (at least at this stage, maybe later?!)

****

Vin

****

Vout

**A.3) Negative feedback, inverting the sign of**

By a rearrangement of node connections in Fig 1 it is possible to apply a negative sign to the gain:  .  
This is called an ‘inverting’ configuration since is out of phase with respect to by 180°   
Keep in mind that for negative feedback, by definition a fraction of must be applied to the terminal of the opamp. However, you are free to cleverly connect to either or

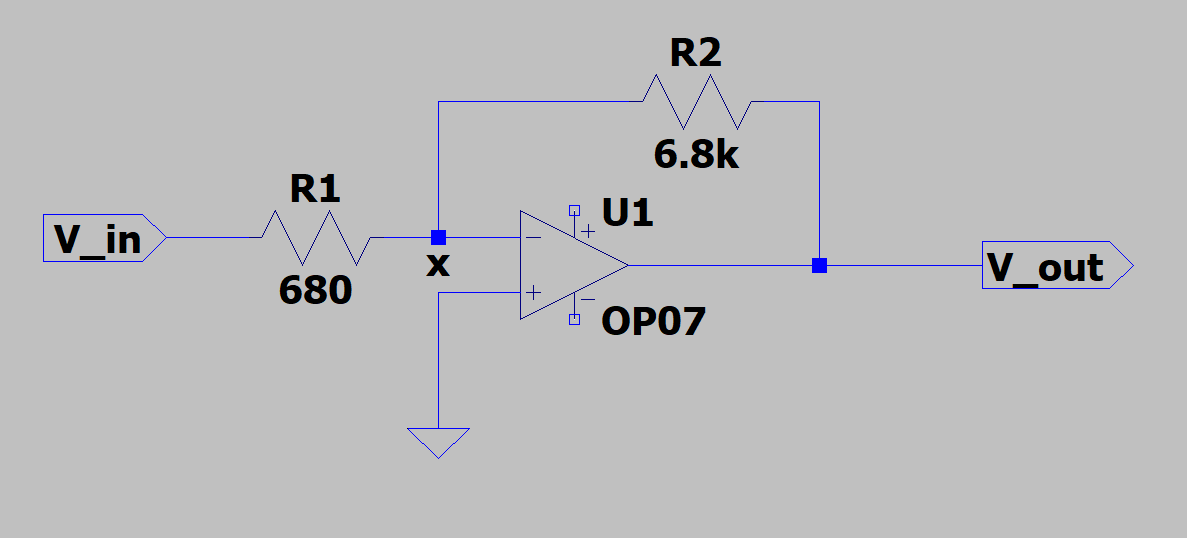
Work out your circuit design and component values for implementing the experimental relation : the absolute value of the is the same, but now there is a negative sign!

**A.3.1) [4]**

Circuit design: **2 marks**

Equations: **1 marks**

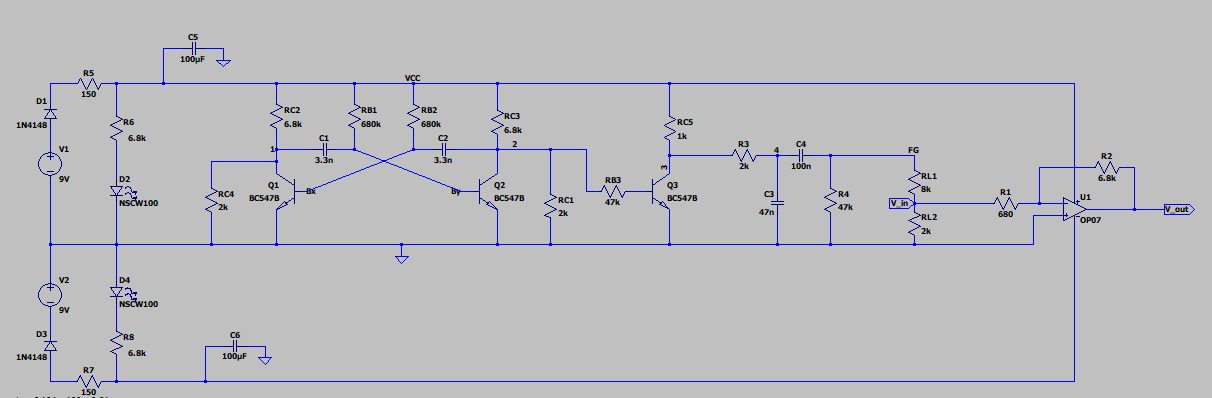
LTSpice simulation: **1 marks**

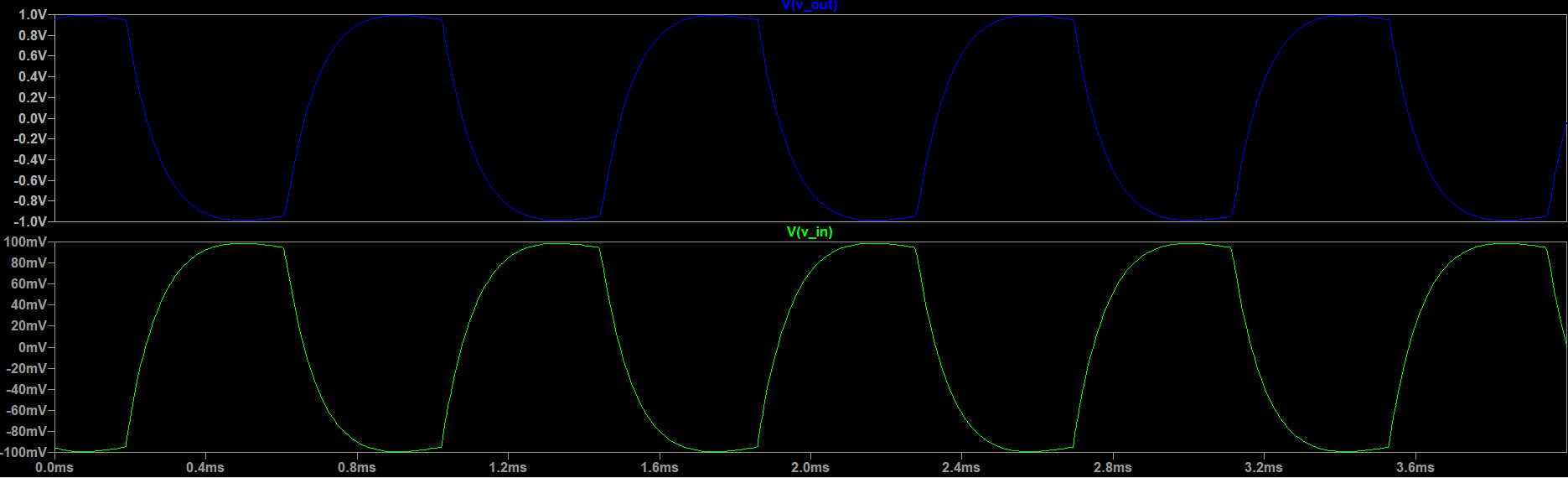


Applying KCL at node x,

Therefore,

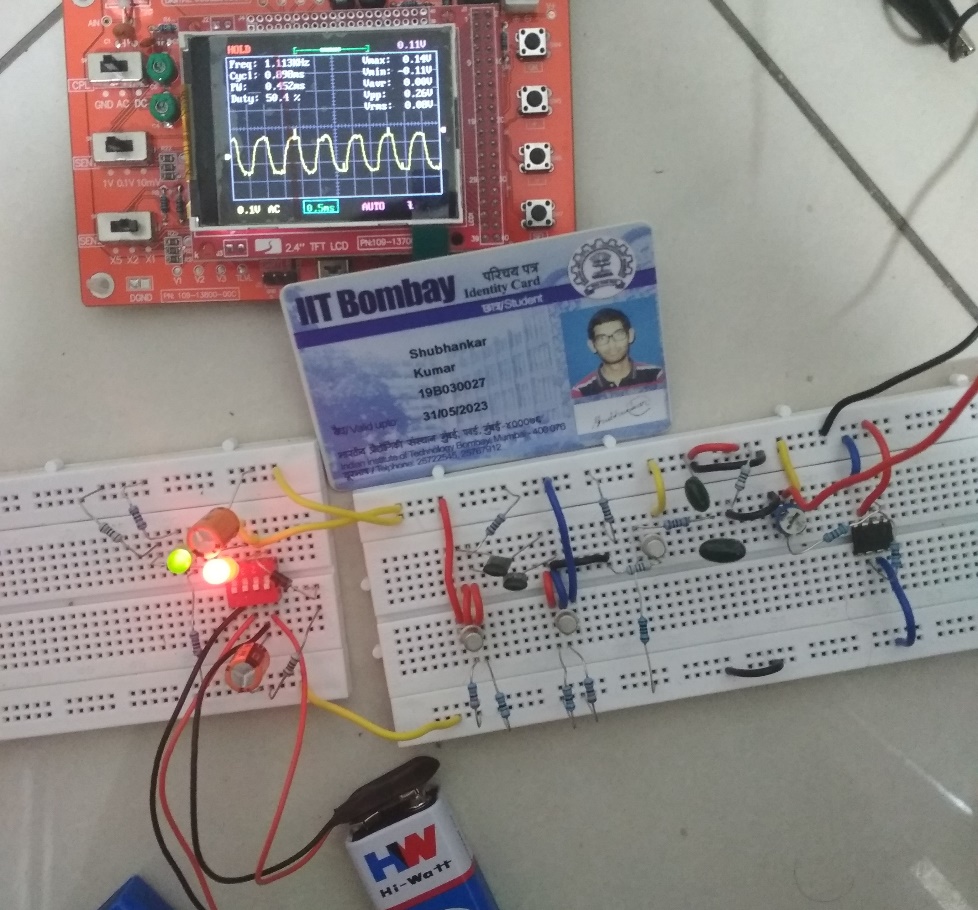
If we want the gain to be -10, then R1 and R2 can be taken as 680Ω and 6.8kΩ respectively.



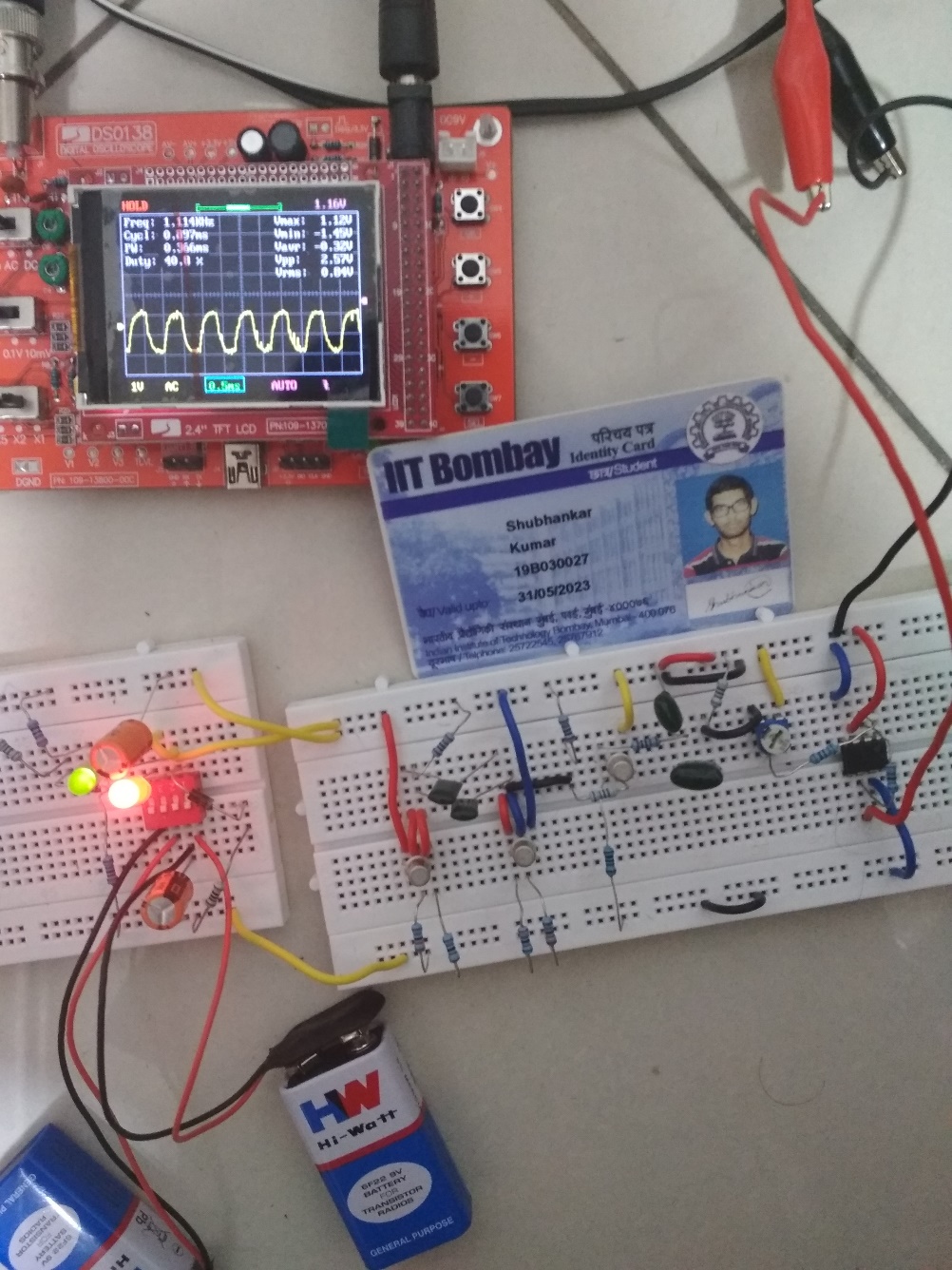
****

**A.3.2) Circuit demo of inverting amplification: [3]**

Build the circuit for inverting amplifier as per A.3.1 and put photos of your working setup.



Vin



Vout

**A.3.3)** With only a single channel measurement on the DSO, how can you tell that the amplifier is inverting the sign of ? It IS possible! **[3]**

(Check the input amplitude Vin being sent from your FG to opamp, and look ahead to question A.4 for a hint)

One way to identify this is the fact that V+ will almost be equal to V- in this case. Hence if we connect the black probe to V+ (ground), the reading should be ~0V when the red probe is connected to V-. Also, since V- is approx. 0V and that the feedback is negative, the output voltage will be negative wrt V-, therefore inverted wrt to Vin.

Another way is to use an “asymmetric” input such as a square wave, say between 0 and 9V. Then the output voltage will range between 0 and a negative number. This will confirm that the output is inverted wrt the input.

**A.4)** **Input impedances?**

**1)** What is the input impedance of the straightforward “non-inverting” configuration of A.1.1, when ? **[2]**

Explain your answer with calculation steps & logical reasoning of the flow of current into/out of various nodes (you can check this in your LTSpice simulation)

The input impedance in this case is generally very high

We have the relation, , where Gf is the closed loop gain, G0 is the open loop gain and Z0 is the input impedance without any feedback.

In this case, Zin = Vin/I. Now since I is extremely small, Zin will be very large. Almost all the current passing through R1 will go to R2.

**2)** What is the input impedance of the “inverting” configuration of A.1.2, when   
? **[2]**

Explain your answer with calculation steps & logical reasoning of the flow of current into/out of various nodes (you can check this in your LTSpice simulation)

In order that the circuit can operate correctly, the difference between the inverting and non-inverting inputs must be very small - the gain of the op amp is very high and therefore for a small output voltage, the difference between the two inputs is small.

This means that inverting input must be at virtually the same potential as the non-inverting one, i.e. at ground. As a result the input impedance of this op amp circuit is equal to the resistor R2 (the input resistance).